

What is claimed is:

1 1. A method for a computer system having a
2 communication link processor and employing a FIFO
3 buffer, comprising the steps of:
4 controlling an asynchronous event storing and
5 recording mechanism by discreet events into the
6 FIFO at a location determined by a write pointer;
7 and
8 causing an attached processor to read the
9 recording mechanism's FIFO at a location determined
10 by a read pointer;
11 said recording mechanism conditionally
12 returning event and status information; and
13 conditionally incrementing the FIFO read
14 pointer.

1 2. The method as recited in claim 1, wherein the
2 fullness indication of the FIFO is returned in the
3 read information as the value of the FIFO read
4 pointer and write pointer.

1 3. The method as recited in claim 1, wherein the
2 recording mechanism returns:
3 system status when the FIFO is completely
4 empty; and
5 an event description when the FIFO has one or
6 more valid entries.

1 4. The method as recited in claim 1, wherein the
2 processor can instruct the recording mechanism to
3 store multiple entries into the processor's main
4 memory.

1 5. The method as recited in claim 4, wherein the
2 said multiple storing of entries from the FIFO does
3 not affect the state of the FIFO read pointer or
4 write pointer.